WHAT IS CLAIMED IS:

1. A method for verifying an integrated circuit device test for testing an integrated circuit device, said method comprising the steps of:

simulating a flawed integrated circuit device comprising one or more known flaws in an integrated circuit device design;

simulating a test of said simulated flawed integrated circuit device; and

determining whether said simulated test of said simulated flawed integrated circuit device discovered said one or more known flaws in said flawed integrated circuit device.

2. A method in accordance with claim 1, further comprising:

modeling said one or more chip defects with said one or more known flaws.

3. A method in accordance with claim 2, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

4. A method in accordance with claim 1, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

5. A method in accordance with claim 1, further comprising the first step of:

generating said integrated circuit device design that meets specifications of said integrated circuit device.

6. A method in accordance with claim 5, further comprising the step of:

verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design.

7. A method in accordance with claim 6, further comprising:

modeling said one or more chip defects with said one or more known flaws.

8. A method in accordance with claim 7, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

9. A method in accordance with claim 1, first comprising the step of:

modifying said integrated circuit device design to include said one or more known flaws to generate said flawed integrated circuit device design.

10. A method in accordance with claim 9, further comprising:

modeling said one or more chip defects with said one or more known flaws.

11. A method in accordance with claim 10, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

12. A method in accordance with claim 9, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

13. A method in accordance with claim 9, further comprising the first step of:
generating said integrated circuit device design that meets specifications of said integrated circuit device.

14. A method in accordance with claim 13, further comprising the step of:
verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design.

15. A method in accordance with claim 14, further comprising:
modeling said one or more chip defects with said one or more known flaws.

16. A method in accordance with claim 15, further comprising the step of:
indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

17. A computer readable storage medium tangibly embodying program instructions implementing a method for verifying an integrated circuit device test for testing an integrated circuit device, said method comprising the steps of:
simulating a flawed integrated circuit device comprising one or more known flaws in an integrated circuit device design;
simulating a test of said simulated flawed integrated circuit device; and

determining whether said simulated test of said simulated flawed
10    integrated circuit device discovered said one or more known flaws in said
flawed integrated circuit device.

18.    The computer readable storage medium of claim 17, further
comprising:

modeling said one or more chip defects with said one or more known
flaws.

19.    The computer readable storage medium of claim 18, further
comprising the step of:

indicating that said test of said simulated flawed integrated circuit
device is flawed if said simulated test of said simulated flawed integrated
5    circuit device does not discover one or more of said known flaws in said
flawed integrated circuit device.

20.    The computer readable storage medium of claim 17, further
comprising the step of:

indicating that said test of said simulated flawed integrated circuit
device is flawed if said simulated test of said simulated flawed integrated
5    circuit device does not discover one or more of said known flaws in said
flawed integrated circuit device.

21.    The computer readable storage medium of claim 17, further
comprising the first step of:

generating said integrated circuit device design that meets
specifications of said integrated circuit device.

22.    The computer readable storage medium of claim 21, further
comprising the step of:

verifying that said test passes simulated good integrated circuit
devices of said generated integrated circuit device design.

23.  The computer readable storage medium of claim 22, further comprising:

modeling said one or more chip defects with said one or more known flaws.

24.  The computer readable storage medium of claim 23, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

25.  The computer readable storage medium of claim 17, first comprising the step of:

modifying said integrated circuit device design to include said one or more known flaws to generate said flawed integrated circuit device design.

26.  The computer readable storage medium of claim 25, further comprising:

modeling said one or more chip defects with said one or more known flaws.

27.  The computer readable storage medium of claim 26, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

28.  The computer readable storage medium of claim 25, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated

circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

29. The computer readable storage medium of claim 25, further comprising the first step of:

generating said integrated circuit device design that meets specifications of said integrated circuit device.

30. The computer readable storage medium of claim 29, further comprising the step of:

verifying that said test passes simulated good integrated circuit devices of said generated integrated circuit device design.

31. The computer readable storage medium of claim 30, further comprising:

modeling said one or more chip defects with said one or more known flaws.

32. The computer readable storage medium of claim 31, further comprising the step of:

indicating that said test of said simulated flawed integrated circuit device is flawed if said simulated test of said simulated flawed integrated circuit device does not discover one or more of said known flaws in said flawed integrated circuit device.

33. An integrated circuit device test verification apparatus, comprising:

an integrated circuit device simulator which simulates a flawed integrated circuit device of an integrated circuit device design;

a tester simulator which simulates a test executing on an integrated circuit device tester that generates test stimuli and receives test responses; and

a simulated test results analyzer which determines whether said simulated test of said simulated flawed integrated circuit device discovered said one or more known flaws in said flawed integrated circuit device.

34. An integrated circuit device test verification apparatus in accordance with claim 33, wherein:

one or more chip defects are modeled with said one or more known flaws.

35. An integrated circuit device test verification apparatus in accordance with claim 34, wherein:

said simulated test results analyzer determines that said test is flawed if said simulated test of said simulated flawed integrated circuit device does not discover said one or more known flaws in said flawed integrated circuit device.

36. An integrated circuit device test verification apparatus in accordance with claim 33, wherein:

said integrated circuit device simulator also simulates a known good integrated circuit device of an integrated circuit device design;

said tester simulator simulates said test executing on said integrated circuit device tester; and

said simulated test results analyzer determines whether said simulated test of said simulated known good integrated circuit device passes said simulated known good integrated circuit device.

37. An integrated circuit device test verification apparatus in accordance with claim 36, wherein:

said simulated test results analyzer determines that said test is flawed if said simulated test of said simulated flawed integrated circuit device does not pass said simulated known good integrated circuit device.